## CLAIMS

1. An integrated circuit, comprising:

a first data processing subsystem including a first processor connected to a first bus as a first bus master;

a second data processing subsystem including a second processor connected to a second bus as a second bus master;

a first slave subsystem including a memory unit, usable by either of the first and second processors, connected to a third bus;

a second slave subsystem, usable by either of the first and second processors, including a fourth bus; and

the first, second, third and fourth buses selectively connected to each other through a bus arbitration module arranged to connect the first and second bus masters to the first and second slave subsystems, respectively, without blocking.

2. The integrated circuit of claim 1, wherein the first slave subsystem further comprises a shared memory connected to the third bus and shared by the first processor and the second processor through the third bus.

3. The integrated circuit of claim 2, further comprising:

a local memory connected to the first processor for communication directly therewith, not through the bus arbitration module.

4. The integrated circuit of claim 3, further comprising:

a direct memory access (DMA) controller; and

a DMA bus connected to the third bus and the fourth bus, whereby data is selectively moved between the first slave subsystem and the second slave subsystem without intervention by the first processor or the second processor.

5. The integrated circuit of claim 4, further comprising:

a memory access interface (MAI) connecting one of the third and fourth buses to the local memory.

6. The integrated circuit of claim 5, wherein the fourth bus includes a connection to an external device.

7. The integrated circuit of claim 6, wherein the external device includes a memory device.

8. A data communications device, comprising:
a communications system having a first internal bus;
a supervision and control system having a second internal bus;
a first slave devices system having a third internal bus;
a second slave devices system having a fourth internal bus; and
a direct memory access (DMA) system having a fifth internal bus;
the first, the second, the third, the fourth and the fifth internal buses interconnected through a bus arbitration module (BAM).

9. The device of claim 8, wherein the first slave devices system further comprises:
system memory accessed by both the data communications system and the supervision and control system through the BAM and the third internal bus.

10. The device of claim 9, wherein the DMA system communicates data directly between the system memory and the second slave devices system.

11. The device of claim 8, wherein the second slave devices system includes system support elements, communication support elements and input/output (I/O) elements.

12. The device of claim 11, wherein the system support elements include an interrupt controller, the communication support elements include global system for mobile (GSM) communications support elements and the I/O elements include a generic serial port.

13. The device of claim 9, wherein the communication system includes a digital signal processor (DSP) connected to the first internal bus.

14. The device of claim 13, wherein the supervision and control system includes a microprocessor control unit (MCU) connected to the second internal bus.

15. The device of claim 14, wherein the DSP and MCU each communicate with an internal device over the first and second internal bus, respectively, and also communicate with the system memory through the BAM and the third internal bus.

16. The device of claim 15, wherein the fourth internal bus includes a connection to an external device.

17. The device of claim 16, wherein the external device includes a memory device.

18. An integrated circuit device used in a telephone handset, the device, in one integrated circuit, comprising:

a digital signal processor (DSP);

a microcontroller unit (MCU);

a shared system memory;

a DSP bus to which the DSP is connected;

an MCU bus to which the MCU is connected;

a peripheral unit and a peripheral bus to which the peripheral unit is connected;

a memory bus to which the shared system memory is connected; and

a bus arbitration module (BAM) which selectively connects the DSP bus and the MCU bus to the memory bus and the peripheral bus, wherein when the DSP and the MCU request access to different buses, access occurs without blocking.

19. The device of claim 18, further comprising:

a direct memory access (DMA) controller and a DMA bus controlled by the DMA controller; wherein

the BAM further selectively connects the DMA bus between the memory bus and the peripheral bus.

20. The device of claim 18, wherein the peripheral unit system includes system support elements, communication support elements and input/output (I/O) elements.

21. The device of claim 20, wherein the system support elements include an interrupt controller, the communication support elements include global system for mobile (GSM) communications support elements and the I/O elements include a generic serial port.

22. The device of claim 18, wherein the DSP and MCU each communicate with a local device over the DSP bus and the MCU bus, respectively, and also communicate with the system memory through the BAM and the memory bus.

23. The device of claim 22, further comprising an external bus including a connection to an external device.

24. The device of claim 23, wherein the external device includes a memory device.

25. A method of prioritizing and granting bus access requests, comprising:

granting the bus access request of a requestor asserting a high priority interrupt;

if no requestor is asserting the high priority interrupt, granting the bus access request of a requestor owning the current request slot; and

if no requestor is asserting the high priority interrupt and no requestor owns the current request slot, granting the bus access request of a requestor highest on a round robin priority list.

26. The method of claim 25, further comprising:

granting access to a processor operating on a real-time signal when the processor has been in a wait state for a time-out period.

27. The method of claim 26, wherein the time-out period is programmable.

28. The method of claim 26, wherein when the processor has been in the wait state for the time-out period, the high priority interrupt is asserted.

29. The method of claim 26, further comprising:

if the request of the requestor owning the current request lot is granted, updating a table of request slot owners.

30. The method of claim 29, further comprising:

if the request of the requestor highest on the round robin priority list is granted, updating the round robin priority list and the table of request slot owners.

31. A programmable device, comprising:

plural master buses;

plural bus masters, each connected to a corresponding one of the plural master buses;

plural slaves buses;

plural resources used by a first one and a second one of the plural bus masters, each of the plural resources connected to a corresponding one of the plural slave buses; and

a bus arbitration module (BAM) interconnecting the plural master buses and the plural slave buses, the bus arbitration module guaranteeing allocation to each of the plural bus masters at least a predetermined number of units of bandwidth for access to the plural resources and that reallocates from a first bus master to which an unneeded unit of bandwidth has been allocated to a second bus master which needs a unit of bandwidth.

32. The device of claim 31, wherein the resource further comprises:

a memory used by at least the first one and the second one of the plural bus masters.

33. The device of claim 31, the BAM further comprising:

a direct memory access (DMA) bus selectively interconnecting two of the plural slave buses.

34. The device of claim 31, wherein the plural resources includes system support elements, communication support elements and input/output (I/O) elements.

35. The device of claim 34, wherein the system support elements include an interrupt controller, the communication support elements include global system for mobile (GSM) communications support elements and the I/O elements include a generic serial port.

36. The device of claim 31, the first bus master further comprising:
a digital signal processor (DSP).

37. The device of claim 36, the second bus master further comprising:
a microprocessor control unit (MCU).

38. The device of claim 37, further comprising an external slave bus including a connection to an external device.

39. The device of claim 38, wherein the external device includes a memory device.